THREE DIMENSIONAL CMOS INTEGRATED CIRCUITS HAVING DEVICE LAYERS BUILT ON DIFFERENT CRYSTAL ORIENTED WAFERS

ABSTRACT OF THE DISCLOSURE

Three-dimensional (3D) integration schemes of fabricating a 3D integrated circuit in which the pFETs are located on an optimal crystallographic surface for that device and the nFETs are located on a optimal crystallographic surface for that type of device are provided. In accordance with a first 3D integration scheme of the present invention, first semiconductor devices are pre-built on a semiconductor surface of a first silicon-on-insulator (SOI) substrate and second semiconductor devices are pre-built on a semiconductor surface of a second SOI substrate. After pre-building those two structures, the structure are bonded together and interconnect through wafer-via through vias. In a second 3D integration scheme, a blanket silicon-on-insulator (SOI) substrate having a first SOI layer of a first crystallographic orientation is bonded to a surface of a pre-fabricating wafer having second semiconductor devices on a second SOI layer that has a different crystallographic orientation than the first SOI layer; and forming first semiconductor device on the first SOI layer.